**ST. ANNE’S**

**COLLEGE OF ENGINEERING AND TECHNOLOGY**

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)

(An ISO 9001: 2015 Certified Institution)

ANGUCHETTYPALAYAM, PANRUTI – 607 106.

**QUESTION BANK**

**PERIOD :** JULY - NOV 2018 **BATCH**: 2015 – 2019

**BRANCH :** ECE **YEAR/SEM:** IV/VII

**SUB CODE/NAME:** EC6009 – ADVANCED COMPUTER ARCHITECTURE

**UNIT I FUNDAMENTALS OF COMPUTER DESIGN**

**PART – A**

1. How the server adapts the dependability characteristics?[ID]
2. Mention the cost of an integrated circuit**.[D][Nov/Dec 2016]**
3. How the server adapts the scalability characteristics? (U)
4. How to find the cost of an integrated circuit**.[ID][Nov/Dec 2016]**
5. What are the five trends in computer architecture**.[D][Nov/Dec 2016]**
6. Define Amdahl’s Law**.[D][Nov/Dec 2017]**
7. If a 20% reduction in voltage leads to 15% reduction in frequency, what would be the impact on dynamic energy and power? **.[D][Nov/Dec 2017]**
8. Define throughput**.[D][Apr/May 2018]**
9. Some microprocessors today are designed to have adjustable voltage. So that a 20% reduction in voltage leads to 15% reduction in frequency, what would be the impact on dynamic power? **.[ID][Apr/May 2018]**
10. Define bandwidth and latency. **[D]**
11. How to predict the number of good chips per wafer**? .[ID]**
12. What are important functional requirements of architecture faces? **[D]**
13. How the performance of the benchmark is measured in real time applications **.[ID]**
14. Write the operating system requirements of a computer. **[D]**
15. Specify the standards required by the market place**. .[ID]**
16. Define Module reliability. **[D]**
17. In what way the volume issues affect the cost wise in super computers **.[ID]**
18. Write about commodities. **[D]**
19. Define Service Level Agreements or Service Level Objectives. **[D][Nov/Dec 2015]**
20. What are the three approaches of source code modifications? **[D]**
21. Discuss about SPEC (Standard Performance Evaluation Corporation**[D][** **Nov/Dec 2015**
22. Define SPEC ratio **[D]**
23. Define geometric mean in SPECR. **[D]**
24. Mention the two important properties of geometric mean. **[D]**
25. Define geometric mean and geometric standard deviation. **[D]**
26. Define Speedup. **[D]**
27. What are the two factors of Amdahl’s Law to find the speedup? **[D]**
28. Write the processor performance equation **[D]**
29. Define clock cycles per instruction (CPI). **[D]**
30. What are the principles of computer design? **[D]**

**PART – B**

**[First Half]**

**[Review of fundamentals of CPU, MEMORY and IO]**

1. Explain briefly about the fundamentals of the processor (8)
2. Discuss briefly about the memory and Input/output interfacing. (16)
3. Discuss the factors that need to be considered while designing the instruction set architecture of a processor(10) **.[D][Nov/Dec 2017]**
4. Explain the recent trends and cost in computer technology. (16)
5. Write short notes on power and energy consumption in a microprocessor. (16)
6. Explain the fundamentals of CPU in modern computer(16)[D]

**[Trends in technology, energy, power and cost]**

1. Write short notes on power and energy consumption in a microprocessor. (16**)[D][Nov/Dec2016]**
2. Explain the recent trends and cost in computer technology. (16)
3. Appraise the major factors that influence the cost of a computer and outline how these factors are changing over time(16)[**D][Apr/May-2018]**
4. What are the major concerns that should be addressed by system architecture with respect to power and energy? Discuss the techniques that commonly employed to address these issues.(10) **ID][Nov/Dec 2017]**
5. Discuss about the cost and commodities in super computers.(8)
6. With an example explain briefly about the quantitative principles (the benchmark) of computer design
7. Explain briefly about the dependability of the processor.

**[Second Half]**

**[Dependability, performance evaluation]**

1. Discuss the performance evaluation methods of different computers(16) **[D][Nov/Dec2016]**
2. Discuss the performance evaluation and explain MTTF,MTTR,MTBR(8**)[D]**
3. Appraise module reliability and module availability with an example(8)[**D][Apr/May-2018]**
4. What are the various performance measures available to evaluate the performance processor? How do each of these relate to the ultimate measure of performance? Explain**.(10)[ID][Nov/Dec 2017]**
5. How to relate the performance of two different computers say, X and Y? Appraise with an example.(8)[**D][Apr/May-2018]**
6. What are the different classes of parallelism and parallel architectures that are available? (6)[**D][Apr/May-2017]**
7. Find the number of dies per 300mm(30)cm wafer for a die that is 1.5cm on a side and for a die is 1.0cm on a side.(7)[D]

**UNIT II-INSTRUCTION LEVEL PARALLISM**

**PART – A**

1. What is Instruction Level Parallelism? **)[D][Nov/Dec 2011])(May/June 2012**)
2. What is loop –level parallelism?[D]
3. What is loop unrolling? and what are the advantages of loop unrolling? **)[D][Nov/Dec 2011]).**
4. what is dynamic scheduling.[D] **May/June 2013**)
5. list the advantages of dynamic scheduling**.[D]( Nov/Dec 2012)(May/June 2012)**
6. Write the 5 levels of branch prediction and define them.[D] **(May/June 2013)**
7. Write the 7 fields of Reservation stations.[D]
8. List the limitations of loop unrolling[D]
9. What is an imprecise exception?[D]
10. What is Branch prediction buffer / Branch history table?[D]
11. List the data hazards in ILP?[D]
12. What is Register Renaming?[D]
13. Write the merits and demerits of software pipelining and loop rolling**[D].(Nov/Dec2012).**
14. What are the advantages and disadvantages of trace scheduling method**?[D](may/June 2012).**
15. Define Software Pipelining (or) Symbolic loop unrolling **(May/June 2012).**
16. Define loop-carried dependence**?[D](May/June 2013).**
17. What are the limitations of VLIW**?[D](Nov/Dec 2011).**
18. What is loop unrolling and what are the major limitation of loop unrolling**?[D](Nov/Dec2012**).
19. Define Loop carried dependence with the example**.[D](May/ June 2013).**
20. What are the advantages and disadvantages of trace scheduling method**?[D](May/June 2012).**
21. What is recorder buffer?[**D][Nov/Dec 2017]).**
22. What is meant by delayed branching?[**D][Nov/Dec 2017]).**
23. What is pipelining?[**D][Nov/Dec 2017]).**
24. Outline the limitations of Instruction Level Parallelism?[**D][Apr/May-2018]**
25. Explain the idea behind dynamic scheduling. **?[D](Nov/Dec 2016).**
26. Give an example for data dependence**? [D](Nov/Dec 2016).**
27. What is loop unrolling? **[D**
28. What are the types of hazards in pipeline? **[D**
29. How is the CPI value calculated for a pipeline processor**[D]**
30. What is score boarding**?[D]**

**PART-B**

**[First half]**

**[ILP concept, pipelining overview, compiler techniques for exposing ILP]**

1. Explain the types of dependencies in ILP(8**)[D] [Nov/dec-2016]**
2. Explain the compilation techniques that can be used to express instruction level parallelism(8) **[D] [Nov/dec-2016]**

**[Dynamic branch prediction, Dynamic Scheduling]**

1. Explain in Dynamic Scheduling. Explain how it is used to reduce data hazards(8**)[D] [Nov/dec-2016]**
2. How data hazards can be overcome withDynamic Scheduling? Appraise with an example **[ID][Apr/May-2018]**
3. Briefly explain how to overcome data hazards with dynamic scheduling using Tomasulo’s approach.(16**)[D] (NOV/DEC 2011, MAY/JUNE 2012, NOV/DEC 2013)**
4. Explain the static and dynamic branch prediction schemes in detail(8**)[D](NOV/DEC 2011,MAY/JUNE 2012, NOV/DEC 2012,MAY/JUNE 2014)**
5. Explain how to Reduce Branch Costs with Dynamic Hardware Prediction. (16) **[D](MAY/JUN2013,APR/MAY 2013)**
6. **Consider the following code:**

LOOP: L.D F2,0(R1)

 MUL,D F4,F2,F0

 L.D F6,0(R2)

 ADD.D F6,F4,F6

 S.D 0(R2).F6

 DADDIU R1,R1,#8

 DADDIU R2,R2,#8

 CMPI R3,R1,#800

 BEQZ R3,LOOP

Assume that there are separate functional units for effective address calculations, for ALU operations and for branch conditions evaluation. Assume latencies for add and 5 for multiply, assume that loads and stores access memory one clock cycle after the effective address calculations. Show the working of this code for two iterations of the loop when executed on a single issue Tomasulo processor that supports speculation.(10)**[ID] [Nov/dec-2017]**

**[Second Half]**

**[Multiple instruction issue]**

1. Write short notes on the different types of multiple issue processors(6)[**D]Nov/dec-2017]**
2. Discuss the various hardware techniques used for handling control hazards (10) **[D][Apr/May-2017]**
3. What is meant by loop unrolling? Discuss the advantages and disadvantages(6) **[D][Apr/May-2017]**
4. Briefly describe any techniques to reduce the control hazard stalls.(16)[**D] (APR/MAY 2011)**
5. Appraise with an example the use of simple compiler technology to enhance a processor ability to exploit instruction level parallelism(16) **[D][Apr/May-2018]**
6. Describe how the compiler technology can be used to improve the performance of instruction level parallelism (16) **[D](APR/MAY 2011,MAY/JUNE 2012)**
7. Briefly explain what are the steps involved in instruction level parallelism.(8)[**D]**

**[Hardware based speculation, static scheduling, multithreading]**

1. Define Multithreading. Explain how ILP is achieved using Multithreading with an example. (8**)[D] [Nov/dec-2016]**
2. Explain hardware based speculation to overcome the control dependencies(16**)[D] (NOV/DEC 2012) (16)**
3. Explain the static and dynamic branch prediction schemes in detail(8)[**D] (NOV/DEC 2011,MAY/JUNE 2012, NOV/DEC 2012,MAY/JUNE 2014)**
4. Briefly describe any techniques to reduce the control hazard stalls.(16**)[D] (APR/MAY 2011)**

 **[Limitations of ILP]**

1. Explain the various limitations of ILP. (16)

**UNIT III DATA LEVEL PARALLELISM**

**PART A**

1. Define data level parallelism. **[D][Apr/May-2018]**
2. How did single core architectures exploit data level parallelism)[I**D] (NOV/DEC2017]**
3. SIMD is preferred over MIMD. Justify it.[ID]
4. What are the types of vector processor?[D]
5. What are the advantages and disadvantages of vector instruction?[D]
6. Define the term Vectorized or Vectorizable.[D]
7. Differentiate MIPS vs VMIPS.[D]
8. Write short notes on convoy.[D]
9. Write code for strip-mined version of the DAXPY loop.[ID]
10. Write short notes on memory banks.[D]
11. State the condition for stalling.[D]
12. Write short notes on SIMD multimedia extensions. **[D][Apr/May-2018]**
13. Differentiate multimedia SIMD and Vector architecture.[D]
14. Write short notes on roofline visual performance model.[D]
15. CUDA will simplify scheduling by hardware justify.[ID]
16. List out the hardware scheduler of GPU.[D]
17. What is mean by warp?[D]
18. Write short notes on Fermi GPU architecture.[D]
19. What is mean by error correcting codes? [D]
20. Define arithmetic intensity.[D]
21. Differentiate GPU and CPU**)[D] [Nov/dec-2016]**
22. List out the primary components of instruction set architecture of VMIPS. **)[D] [Nov/dec-2016]**
23. Differentiate vector architecture and GPUs.[D]
24. What is mean by warp scheduler?[D]
25. Write short notes on SIMD lane and Thread processor.[D]
26. Define recurrence with example.[D]
27. Write short notes on dependence analysis.[D]
28. Is there any reason for requirement of substantial memory by GPU.[ID]
29. Define the term reduction.[D]
30. List out the primary components of instruction set architecture of VMIPS**.[D] [NOV/DEC-2016]**
31. Ude GCD test to identify if loop-carried dependency exists for the following loop:for(i=1;i<=100;i++]

{A[3\*i+5]=A[5\*i+8]\*7;}[ID] **[NOV/DEC2017]**

1. What is SIMD?[ **D][Apr/May-2018]**
2. What are the properties of vector processor?**[D]**

**PART-B**

**[First half]**

**[Vector architecture]**

1. Explain about VIMPS vector architecture.[D] (16)
2. Discuss similarities and difference between vector architecture and GPUs**.(16)[D][ Nov/Dec-16]**
3. Explain VMIPS vector instruction set in detail.16 **[D]**
4. Discuss the salient features of vector processor(10**)[D] [NOV/DEC2017]**
5. How do youdetermine the execution time of a sequence of vector operations? explain with example.**(6)[ID] [NOV/DEC2017]**
6. What is meant by gather-scatter? How it handles sparse matrices in vector architecture?(8) **[ID]**
7. Explain memory for supplying bandwidth for vector load/store units. (16**)[D]**
8. Explain with a diagram the basic structure of a vector processor.(16)[**ID] [NOV/DEC2017]**
9. With an example explain how vector length register handles a loop when it is not equal to 64.( 8**)[ID]**
10. Explain in detail about roofline visual performance model.( 8**)[D]**

**[SIMD extensions]**

1. Explain multithreaded SIMD processor. (8)

Identify the true dependences, output dependences and anti dependences in the code given below and eliminate the name dependences through register renaming.(6**)[ID][NOV/DEC2017]**

For(i=0;i<100;i=i+1){

Y[i]=X[i]/c\*S1\*/

X[i]= X[i]+c;/\*S2\*/

Z[i] = X[i]+c;/\*S3\*/

Y[i]=c-Y[i];/ \*S4\*/

}

 **[Second half]**

**[Graphic processing units]**

1. Present an outline of graphical processing units**(8)** [ **D][Apr/May-2018]**
2. What are the architectural features that distinguish a GPU from a normal CPU? Discuss with a case study.(10**)[ID] NOV/DEC2017]**
3. Define GPU. Explain how programming can be performed in GPU with an example. (8)[**ID]**
4. Explain PTX GPU instruction set in detail. (16**)[D]**
5. Discuss about GPU memory structure. (10)[D]
6. Explain in detail about Fermi GPU structure.(6)

**[Loop level parallelism]**

1. Explain detecting and enhancing loop level parallelism in detail.(16**)[D] (Nov/Dec-2016)**
2. Explain loop level parallelism with an example.(8) [ **D][Apr/May-2018]**

**UNIT IV THREAD LEVEL PARALLELISM**

**PART A**

1. Define Thread and Thread-level parallelism (TLP)?[D]
2. What are the two different types of parallel structure in thread level parallelism?[D]
3. Thread-level parallelism is an important alternative to instruction-level parallelism-Justify.[ID]
4. List the major MIMD Styles. What are the advantages of MIMD multiprocessor? [D]**(Nov/Dec-13)**
5. What are the challenges in parallel processing?[ID]
6. What do you understand by grain size? What is its impact on parallelism?
7. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential?[ID]**(Nov/Dec-14)**
8. What are the advantages and disadvantages of using symmetric shared memory? [D]**(May/June-13)**
9. Why Symmetric Shared memory architecture is called as UMA?[D]
10. Define multiprocessor cache processor.[D] **(May/June-12) (Apr/May-15)**
11. What do you understand by Cache coherence Problem? Give an example.[ID]
12. When can we say that the memory is coherent in a multi-processor system? [ID]**(May/June-14)**
13. What is known as coherence missing?[D]
14. What are the four components in execution time?[D]
15. Why do we need synchronization?[D][ **(MAY/JUNE-14)**
16. Define atomic exchange.
17. What is meant by consistency? **(MAY/JUNE-13)**
18. What is the importance of memory consistency model**?[D] (Nov/ Dec-13)**
19. Define consistency memory model**?[D](Nov/Dec-12)**
20. Distinguish between shared memory multiprocessor and message passing multiprocessor?**[D](Nov/Dec-12)**
21. List the methods for providing synchronization in threads[D] **[Nov/dec-2016]**
22. Define Causal consistency memory model.[D] **(Nov/Dec 2012) (K)**
23. What is simultaneous multithreading (SMT)?[D] (Nov/Dec -12) (Nov/Dec-14 )
24. Enlist the features of SMT architecture.[D] (Apr/May-15)
25. Write the benefits of multi core architecture.[D] (May/June-14)
26. Why design issues of SMT and CMT architectures are important?[D] (May/June-14)
27. List the methods for providing synchronization in threads [D] **[Nov/dec-2016]**
28. Define sequential consistency. [D] **[Nov/dec-2016]** [D] **[Nov/dec-2017]**
29. What is meant by false sharing? [D] **[Nov/dec-2017]**
30. Define process and a Thread. [ **D][Apr/May-2018]**
31. What is a chip multiprocessor? [ **D][Apr/May-2018]**

**PART-B**

**[First half]**

**[Symmetric and distributed shared memory architectures]**

1. Described distributed shared memory architecture in detail(16) [D] **[Nov/dec-2016]**
2. Briefly compare instruction level parallelism with thread level parallelism.(8)[D]
3. What is multiprocessor? Explain with a diagram the basic structure of a symmetric shared memory multiprocessor.(8)[D][**Apr**/**May2018**]
4. With neat block diagram explain the centralized shared memory multiprocessor architecture. (16)[**D**] [Nov/Dec 2012)
5. With neat block diagram explain the centralized shared memory multiprocessor architecture.(16)[D](Nov/Dec 2012)
6. Explain the directory–based cache coherence protocol in distributed shared memory architecture.(16)[D] (Nov/Dec-13,16)
7. Discuss the performance of Symmetric Shared-Memory Multiprocessors for a multi-programmed workload consisting of both user activity and OS activity.(16)[D] (May/June-12 ) (Apr/May -15).
8. Discuss the various cache-coherence protocols used in symmetric shared memory architecture.(8)[D] (May/June-12).
9. Explain the concept of simultaneous Multi Threading(6)[D][Nov/Dec2017]

**[Performance issues , Synchronization]**

1. What are the hardware primitives available to resolve synchronization issues in a multiprocessor environment? Give examples.(8)[D] (Nov/Dec-13) (May/June-12).
2. Explain how to implement synchronization in a multiprocessor using a set of hardware primitives with the ability to automatically read and modify a memory locatin. (8)[D][May/Jun2018]

[**Models of memory consistency]**

1. Explain various memory consistency models in detail.(16)[D] (May/June-12, 13) (Nov/Dec-13, 14, 16) (Apr/May-15)
2. What do you mean by snooping protocol? Explain how it is used to maintain the coherence. (8) [D]
3. Explain the snoop based cache coherence protocol with a state diagram.(10) [D][Nov/Dec2017]
4. How are spin locks implemented using cache coherence?(6)[D][Nov/Dec2017]

[**Case studies Intel i7 processor, SMT and CMP processors]**

1. Discuss the design challenges of SMT architecture.(8)[D] (Nov/Dec-13) (May/June-13).
2. Explain Intel multi core architecture with its benefits. (8)[D]
3. Explain in detail about the CMP architecture and its performance.(16)[D] (Nov/Dec- 13-14).
4. Compare and contrast Intel multi core architecture and SUN CMP architecture.(16)[D](Apr/May-15).
5. Discuss the silent features of the Intel i7 processor(10)[D][Nov/Dec2017]

**UNIT 5 MEMORY AND I/O**

**PART A**

1. List the basic optimization techniques of cache.[D][Nov/Dec2016]
2. What are the types of storage devices?[D][Nov/Dec2016]
3. Define the term reliability and availability.[D][Nov/Dec2017]
4. Point out one simple techniques used to reduce each of the three ‘C’ misses in cache memories.[ID][Nov/Dec2017]
5. Outline the difference between volatile memory and non volatile memory.[ID][May/Jun2018]
6. Define cache Hit and cache Miss[D][May/Jun2018]
7. Define the terms cache miss and cache hit.[D] (Nov/Dec 2011) (May/June 2013)
8. What do you mean by write through cache and write back cache?[ID](April/May 2011)
9. What are the categories of cache organization based on placing a block?[D] (Nov/Dec 2013)
10. State the principle of locality.[D] (May/June 2014)
11. List the types of locality[D] (May/June 2014)
12. Write about memory hierarchy.[D]
13. Show the multilevel memory hierarchy with speed and size.[ID]
14. What is branch straightening?[D]
15. Define i) local miss rate ii) global miss rate[D]
16. Define the terms: access time, bandwidth (May/June 2014)[D]
17. Compare SRAM with DRAM[D]
18. How to improve the memory Bandwidth?[D]
19. What is flash memory?[D]
20. Give the comparison between flash and disk.[D]
21. What is the average time to read or write a 512 byte sector for a disk? The advertised average seek time is 5ms, the transfer rate is 40 MB/second, it rotates at 10000 RPM, and the controller overhead is 0.1ms. Assume the disk is idle so that there is no queuing delay.[ID] (May/June 2012)
22. What is the bus master?[D] (May/June 2013)
23. What is CPU- memory bus?[D]
24. Compare software and hardware RAID.[D](Nov/Dec 2012)
25. Define MTTR ii) MTTF.[D]
26. What is RAID?[D](Nov/Dec 2011)
27. How the row diagonal parity works?[D]
28. Define dependability.[D]
29. Define faults, errors, failures. Give example.ID]
30. Give the relation between faults, errors and failures.[D]
31. What do you mean by service specification?[D]
32. How to improve the reliability?[ID]

**PART B**

**[FIRST PART]**

 **[Cache Performance , Reducing Cache Miss penalty and Miss Rate , Redusing Hit time]**

1. Explain the categories of misses and how will you reduce cache miss rate(16)[DN][Nov/Dec2016]
2. Explain the various techniques available for reducing cache miss rate**.(16)[D] (May/June 2012)(Nov/Dec 2013]**
3. Explain the categories of misses and how will you reduce cache miss rate. (16)[D](Nov/Dec 2016).
4. Discuss any five advanced cache coherence protocol with a stated diagram(10)[D][Nov/Dec 2018]
5. Suppose that in 1000 memory reference there are 50 misses in the first level cache and 20 misses in the second level cache. What are the various miss rate? Assume the miss penalty from the L2 cache to memory is 100 clock cycles the hit time of the L2 cache is 10 clock cycles. The hit time of L1 is1 clock cycle and there are 2 memory references per instruction. What is the average memory access time?(6)**[ID][Nov/Dec2017]**
6. Discuss the various techniques available for reducing cache miss penalty.(16)**[D] (May/June2012,14,16**)
7. Explain the various hit time reduction technique.(16)[D**] (Nov/Dec 2013**)
8. Explain with an example any two techniques for improving the cache performance by reducing the miss rate(16)[**D][May/Jun2018]**

**[SECOND PART]**

**[Main memory and performance, Memory technology, Types of storage devices]**

1. Discuss the concept of virtual memory and explain how a virtual memory system is implemented , pointing out the hardware and software support(10)[**ID][Nov/Dec2017]**
2. Explain in detail about main memory and its performance. (16**)[D]**
3. Briefly explain the types of storage devices(8**).[D] (May/June 2014)**
4. Discuss in detail about Virtual memory. (8)[D]
5. Explain in detail about memory technology.(8)[D]

**[ Buses , RAID – Reliability, Availability and Dependability]**

1. Explain the various levels of RAID.(16)[**D] (May/June 2013,14) (Nov**/**Dec** **2012,13,]**
2. Explain about reliability, availability and dependability. (8)
3. Describe about bus. (8)[D]
4. Discuss the different levels of RAID technology , listing their advantages and disadvantages . (6)[**D**] [**Nov**/**Dec2017**]
5. Explain the Bus standards and the interfaces, with timing diagrams. Explain the read and write operations occurring in a typical bus. (16)[D]

**[I/O Performance Measures]**

1. Discuss in detail about various I/O performance measures.(16)[**D] (May**/**June** **2013, 14) (Nov/Dec 2016).**
2. Explain the various of measure I/O performance(8**)[D][Nov/Dec2016**]

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